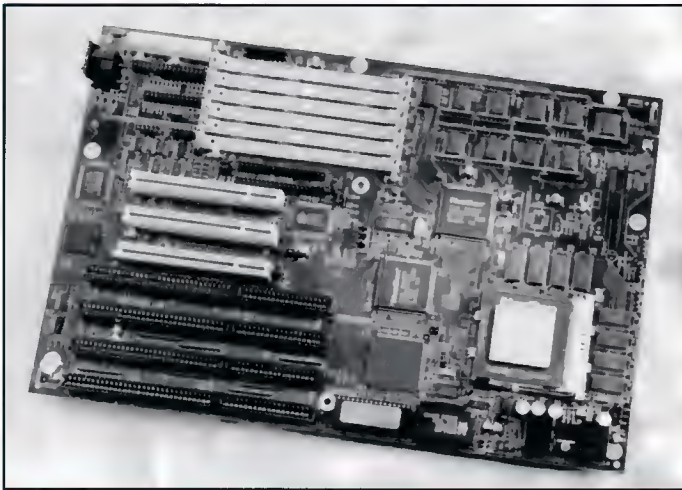


NxPCI BABY - AT MOTHERBOARD ADVANTAGES



■ FAST

PCI, integrated bus mastering IDE, and a high-end memory subsystem push 5th generation performance to new heights.

■ COMPATIBLE

Fully x86 compatible. Microsoft® Windows™ Compatible; Ready to Run™ with OS/2™; *Yes, It Runs with Netware®. Certified by XXCAL independent testing laboratories.

■ INTEGRATED

Fast PCI bus master IDE, on-board floppy controller, 2 serial ports (16550 compatible), 1 enhanced parallel port.

■ AFFORDABLE

Priced to make Nx586 processors the price/performance leader.

KEY ENHANCEMENTS OF NxPCI AND TRITON

■ Fast Bus Master IDE

This advanced interface provides a high performance data path between IDE and PCI peripherals. The bus mastering enhancement gives the IDE controller the capability to initiate data transfers without the help of the CPU, thus freeing up the processor for other activities.

■ High Performance Memory Subsystem

NxPCI and NxMC™ support up to 768 MB Main Memory (EDO or fastpage) and utilize a deep write buffer and dual stream read prefetch buffer to improve memory performance.

■ Support for EDO Memory

EDO is the newest form of high-speed RAM which is better than conventional DRAM at keeping up with high speed processors and PCI bus mastering devices, thus reducing wait states - the time a CPU sits idle waiting for data from memory.



KEY NxPCI/Nx586 ENHANCEMENTS - NOT IN TRITON

■ Supports Parity Checking

Parity checking is essential for catching bit errors in main memory.

■ Enhanced Buffering Scheme

Increased depth of NxPCI buffers provides extended bus bandwidth.

■ 4-Way Set Associative L2 Cache Organization

Triton provides only a direct mapped organization. Nx586 on-board L2 set associativity improves the L2 cache hit rate.

■ Greater DRAM Range and Capacity

NxPCI Capacity: 2-768 MB Triton: 4-128 MB

■ Better IDE Transfer Rate Potential

NxPCI potential: 33 MB/sec Triton: 22 MB/sec

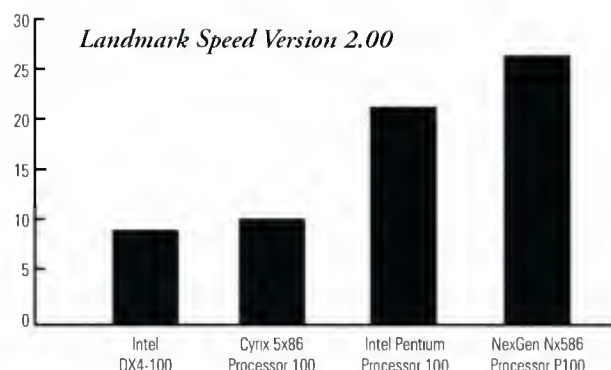
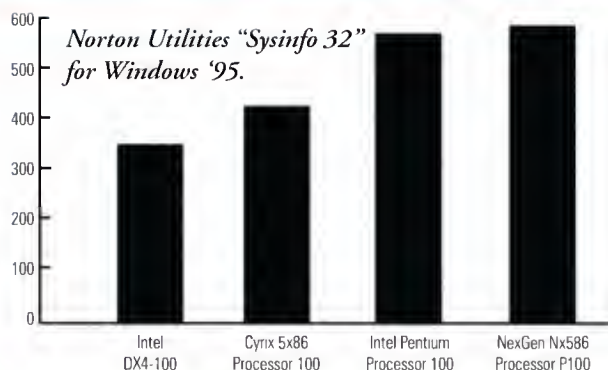
■ Higher L2 Cache SRAM Capacity

NxPCI: 256K or 1MB Triton: 0K, 256K, or 512K

■ L2 Cache Control on Nx586

Ensures the level two cache will always run at full performance and lowers PC costs by allowing the Nx586 processor to run at full speed with slower - and less expensive - cache memory.

PERFORMANCE DATA



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■ INTEGRATED L2 CACHE CONTROLLER

Cache Organization
Write-Back Cache Policy
MESI Protocol Support
SRAM Capacity
SRAM

TRITON
82430FX PCIset
x
Direct Mapped ONLY
x
x
0 - 512K
Sync Pipelined

NxPCI
SYSTEM LOGIC
Integrated on Nx586
4-way set associative
x
x
256K - 1MB
Async or Sync Flow-Through

■ INTEGRATED DRAM CONTROLLER

Parity Support
64-Bit Data Path to Memory
DRAM Capacity
RAS Lines
Buffer Depth for Write Cycles
DRAM Voltage Support
EDO Memory Support
Autodetection of SIMMs

x
x
4 MB - 128 MB
5
4 Qword
3V and 5V
x
x

x
x
2 MB - 768 MB
6
8 Qword
5V
x
x

■ FULLY SYNCHRONOUS 25/30/33 MHZ PCI BUS INTERFACE

Greater than 100 MB/sec PCI Data Streaming
CPU-Memory Bandwidth
Synchronized CPU-to-PCI Interface for High Performance Graphics
PCI Bus Arbiter: 4 Bus Master Support
CPU-to-PCI Memory Write Buffer
Converts Back-to-Back Sequential CPU to PCI Memory
Writes to PCI Burst Writes
PCI-to-DRAM Buffer
Bus Masters Supported
PCI-to-DRAM Bandwidth

x
x
230 MB/sec
x
x
16 byte
x
48 bytes
5
120 MB/sec
Utilizes "Snoop Ahead" x
Sync, Async & Divided Synch
x
260 MB/sec
Sync, Async & Divided Synch
x
32 byte
x
128 bytes
5
120 MB/sec
Utilizes "64 byte buffer prefetch"

■ PCI/ISA BRIDGE

x x

■ PCI/ISA MASTER/SLAVE INTERFACE

PCI from 25-33 MHz
ISA from 7.5-8.33 MHz
ISA Slots

x
x
5 x
x
5

■ FAST IDE INTERFACE

PIO and Bus Master IDE
Mode 4 Timing Support
Transfer Rate Potential
Buffer for Bus Master IDE PCI Burst Transfers

x
x
22 MB/sec
32 byte x
x
33 MB/sec
64 byte

Plug-n-Play Port for Motherboard Devices
Steerable PCI Interrupts for PCI Device Plug-n-Play

x
x x
x

■ CHIPSET PACKAGES

Triton Sytem Controller
Triton Data Path (1)
Triton Data Path (2)
PCI ISA IDE Xcelerator

NxPCI System Logic
NxMC Memory Controller
PCI/ISA Bridge
Symphony Sonata
PCI-IDE Controller